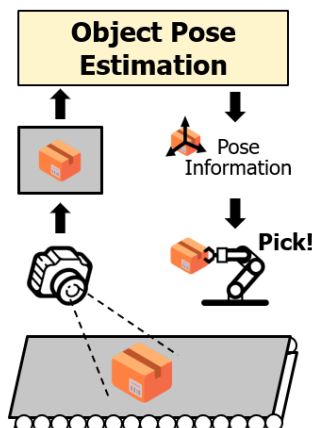


Prediction-Guided Heterogeneous Architecture for Ultra-Low-Latency 3DoF Object Pose Estimation

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Background

Object Pose Estimation in Factory Automation:

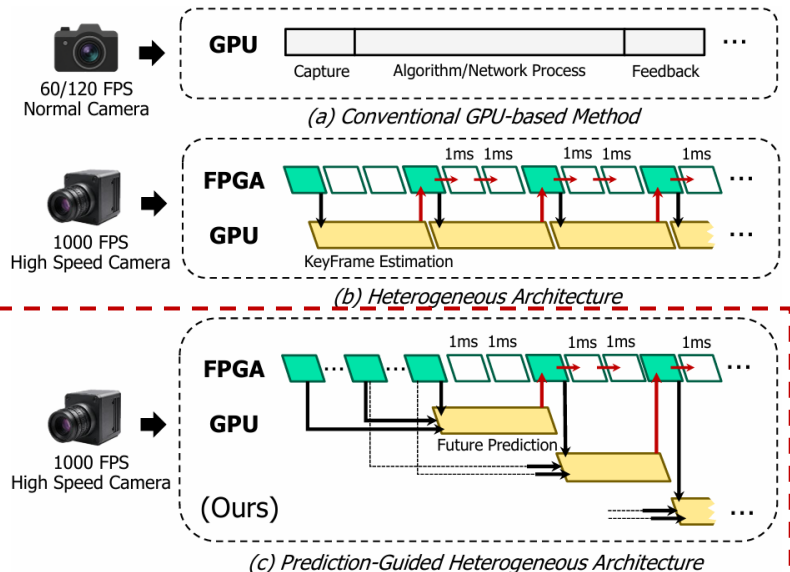


Previous architecture:

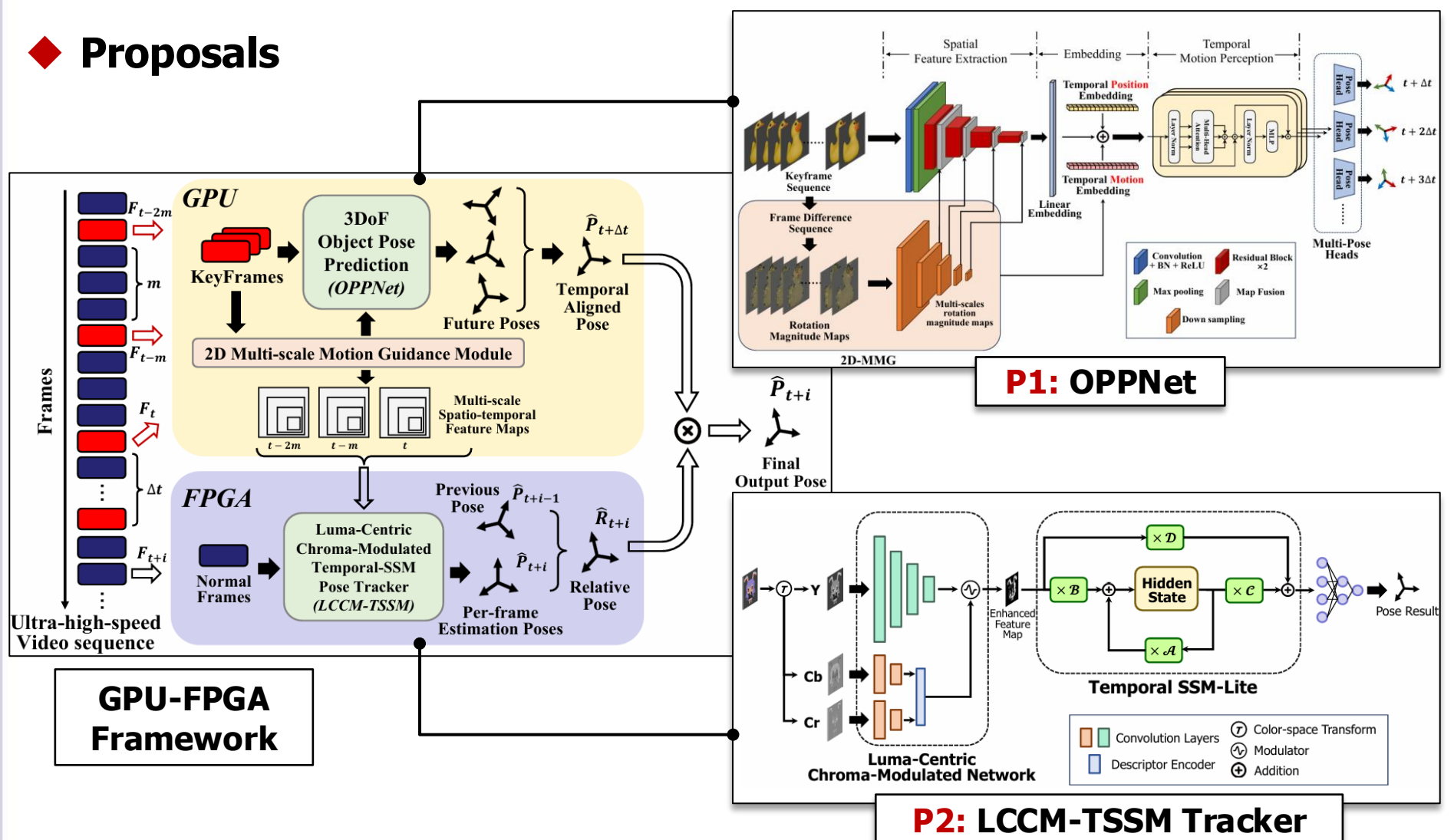
- GPU inference delay cause output misalignment problem and the accuracy drops.
- FPGA implement a rule-based method which is lack of adaptability.

Prediction-guided (My):

- Use prediction to compensate for the GPU's delay.
- Lightweight pose tracker which can automatically learn temporal information.



Proposals



Experiment Results

FPGA Board: ZCU104

Methods	Metrics	QAE (mean) ↓	ADD-0.1d ↑	ADD-0.05d ↑
Wang's work		8.03	98.3%	82.7%
OPPNet (basic)		15.01	88.5%	70.6%
OPPNet + P1.1		8.91	95.3%	82.3%
OPPNet + P1.2		8.03	98.3%	82.7%
OPPNet + P1.1 + P1.2		5.37	99.7%	94.1%

Item	Utilization
Resource Utilization	# LUT: 54709 (23.75%)
	# FF: 103944 (22.56%)
	# DSP: 278 (16.09%)
	# BRAM: 100.5 (32.21%)
Performance	Frequency: 100 MHz
	Processing Time: 0.929 ms/frame

Conclusion

- The proposed system achieves SOTA result of real-time pose estimation.
- Processing time per frame is within an ultra-low-delay of 0.929ms.

